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LISTING OF CLAIMS

1. (Canceled)
2. (Currently amended) A microdevice for forming a part of an integrated circuit, comprising:
a first conductive region and a second conductive region having a channel region interposed therebetween; and
a channel region controlling component disposed over the channel region and separated therefrom by at least one dielectric layer, wherein the channel region controlling component has a non-linear structural characteristic derived from a non-linear structural characteristic of a photo resist feature used as an etch mask for the channel region controlling component.
~~The microdevice according to claim 1,~~ wherein the non-linear characteristic of the photo resist feature provides mechanical stability to the photo resist feature.
3. (Original) The microdevice according to claim 2, wherein the non-linear characteristic of the photo resist feature includes an arc.
4. (Original) The microdevice according to claim 2, wherein the non-linear characteristic of the photo resist feature includes a vertex.
5. (Original) The microdevice according to claim 2, wherein the non-linear characteristic of the photo resist feature includes a tab extending laterally beyond a width of the photo resist feature.
6. (Original) The microdevice according to claim 2, wherein the channel region controlling component is made by deconstructive patterning of one of the photo resist feature or a structure patterned using the photo resist feature.

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7. (Original) The microdevice according to claim 2, wherein the microdevice is a transistor, the channel region controlling component is a gate electrode, the first conductive region is a source and the second conductive region is a drain.

8. (Original) The microdevice according to claim 7, wherein at any point measured generally perpendicular to a bisector of the gate electrode, the gate electrode has a generally constant dimension.

9. (Original) The microdevice according to claim 8, wherein a gate length is defined by the generally constant dimension.

10. (Original) The microdevice according to claim 8, wherein the generally constant dimension is one of a physical dimension or an electrical dimension.

11. (Original) The microdevice according to claim 2, wherein the microdevice is a flash memory device, the channel region controlling component is a word line and the first and second conductive regions are bit lines.

12. (Original) The microdevice according to claim 11, wherein the flash memory device is a dielectric charge trapping flash memory device.

13. (Original) A method of fabricating a microdevice for an integrated circuit, comprising:

providing a wafer having a photo resist layer disposed over an underlying layer;
exposing and developing the photo resist layer to form a photo resist feature having a non-linear structural characteristic, the non-linear characteristic of the photo resist feature providing mechanical stability to the photo resist feature; and

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etching the underlying layer to form a component of the microdevice from the underlying layer, the component having a non-linear structural characteristic corresponding to the non-linear characteristic of the photo resist feature.

14. (Original) The method according to claim 13, wherein the non-linear characteristic of the photo resist feature includes an arc.

15. (Original) The method according to claim 13, wherein the non-linear characteristic of the photo resist feature includes a vertex.

16. (Original) The method according to claim 13, wherein the non-linear characteristic of the photo resist feature includes a tab extending laterally beyond a width of the photo resist feature.

17. (Original) The method according to claim 13, wherein the component of the microdevice is a channel region controlling component and the method further includes deconstructive patterning of one of the photo resist feature or a structure patterned using the photo resist feature as part of forming the component.

18. (Currently amended) The method according to claim 13, wherein the microdevice is a transistor, the component is a gate electrode of the transistor, ~~[[the]]~~ a first conductive region is a source and ~~[[the]]~~ a second conductive region is a drain.

19. (Original) The method according to claim 18, wherein at any point measured generally perpendicular to a bisector of the gate electrode, the gate electrode has a generally constant dimension, the generally constant dimension defining a gate length.

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20. (Original) The method according to claim 19, wherein the generally constant dimension is one of a physical dimension or an electrical dimension.

21. (Currently amended) The method according to claim 13, wherein the microdevice is a flash memory device, the component is a word line and [[the]] first and second conductive regions are bit lines.